



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rajski et al.

Application No. 09/620,021

Filed: July 20, 2000

Confirmation No. 3823

For: CONTINUOUS APPLICATION AND
DECOMPRESSION OF TEST PATTERNS
TO A CIRCUIT-UNDER-TEST

Examiner: Phung M. Chung

Art Unit: 2133

Attorney Reference No. 1011-54375-01

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Attorney or Agent
for Applicants

Date Mailed

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INFORMATION DISCLOSURE STATEMENT PURSUANT TO
37 C.F.R. § 1.97(c)

Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language documents. Applicants respectfully request that these documents be listed as references cited on the issued patent. This Information Disclosure Statement ("IDS") is being mailed before Applicants received a final action, a notice of allowance, or an action that otherwise closes prosecution in the referenced application.

Copies of United States patents and United States published patent applications do not have to be provided to the Patent Office (37 C.F.R. 1.98(a)(2)(ii)). Copies of unpublished U.S. applications do not have to be provided, as long as the application is available on PAIR, as this requirement of 37 C.F.R. § 1.98(a)(2)(iii) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on October 19, 2004 (1287 OG 163). Applicants will provide copies of such patents or applications upon request.

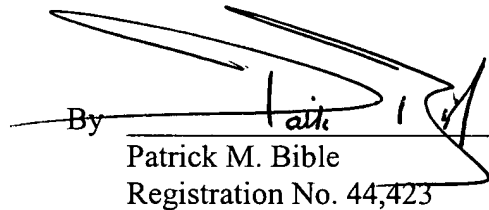
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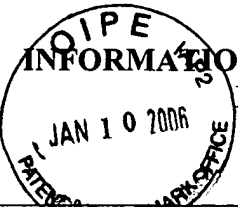
Respectfully submitted,

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Docketing

	Attorney Docket Number	1011-54375-01
	Application Number	09/620,021
	Filing Date	July 20, 2000
	First Named Inventor	Rajski
	Art Unit	2133
Examiner Name		Phung M. Chung

U.S. PATENT DOCUMENTS

Copies of U.S. Patent documents do not need to be provided, unless requested by the Patent and Trademark Office. For patents, provide the patent number and the issue date. For published U.S. applications, provide the publication number and the publication date. For unpublished pending patent applications, provide the application number and the filing date.

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
		6,272,653	8.27.2001	Amstutz
		6,308,291	10.23.2001	Kock et al.

FOREIGN PATENT DOCUMENTS

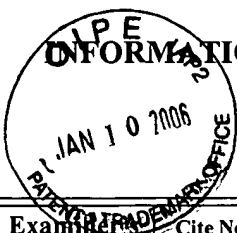
Examiner's Initials*	Cite No. (optional)	Country	Number	Publication Date	Name of Applicant or Patentee

OTHER DOCUMENTS

Examiner's Initials*	Cite No. (optional)	
		Aitken et al., "A Diagnosis Method Using Pseudo-Random Vectors Without Intermediate Signatures," <i>Proc. ICCAD</i> , pp. 574-577 (1989).
		Bardell et al., <u>Built-In Test for VLSI Pseudorandom Techniques</u> , Chapter 4, "Test Response Compression Techniques," John Wiley & Sons, Inc., pp. 89-108 (1987).
		Benowitz et al., "An Advanced Fault Isolation System for Digital Logic," <i>IEEE Transactions on Computers</i> , Vol. C-24, No. 5, pp. 489-497 (May 1975).
		Chakrabarty et al., "Optimal Zero-Aliasing Space Compaction of Test Responses," <i>IEEE Transactions on Computers</i> , Vol. 47, No. 11, pp. 1171-1187 (November 1998).
		Chakrabarty, "Zero-Aliasing Space Compaction Using Linear Compactors with Bounded Overhead," <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , Vol. 17, No. 5, pp. 452-457 (May 1998).

EXAMINER SIGNATURE:	DATE CONSIDERED:
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* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.

		Attorney Docket Number	1011-54375-01
		Application Number	09/620,021
		Filing Date	July 20, 2000
		First Named Inventor	Rajski
		Art Unit	2133
		Examiner Name	Phung M. Chung
Examiner Initials*	Cite No. (optional)	OTHER DOCUMENTS	
		Ghosh-Dastidar et al., "Fault Diagnosis in Scan-Based BIST Using Both Time and Space Information," <i>Proc. ITC</i> , pp. 95-102 (September 1999).	
		Karpovsky et al., "Board-Level Diagnosis by Signature Analysis," <i>Proc. ITC</i> , pp. 47-53 (1988).	
		Karpovsky et al., "Design of Self-Diagnostic Boards by Multiple Signature Analysis," <i>IEEE Transactions on Computers</i> , Vol. 42, No. 9, pp. 1035-1044 (September 1993).	
		Kundu, "On Diagnosis of Faults in a Scan-Chain," <i>Proc. VLSI Test Symp.</i> , pp. 303-308 (1993).	
		Narayanan et al., "An Efficient Scheme to Diagnose Scan Chains," <i>Proc. ITC</i> , pp. 704-713 (1997).	
		Rajski et al., <u>Arithmetic Built-In Self-Test for Embedded Systems</u> , Chapter 3, "Test Response Compaction," and Chapter 4, "Fault Diagnosis," Prentice Hall PTR, pp. 87-133 (1998).	
		Rajski et al., "Diagnosis of Scan Cells in BIST Environment," <i>IEEE Transactions on Computers</i> , Vol. 48, No. 7, pp. 724-731 (July 1999).	
		Saluja et al., "Testing Computer Hardware through Data Compression in Space and Time," <i>Proc. ITC</i> , pp. 83-88 (1983).	
		Wu et al., "Scan-Based BIST Fault Diagnosis," <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , Vol. 18, No. 2, pp. 203-211 (February 1999).	

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